

Effects of Heavy Ion Exposure on Nanocrystal Nonvolatile Memory

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Abstract—Advanced nanocrystal nonvolatile memories have been exposed to heavy ion bombardment. They appear to be promising candidates for future spacecraft electronics.

Index Terms—Component, electronics, nanocrystals, nonvolatile memory, radiation effects.

I. INTRODUCTION

WE have irradiated engineering samples of Freescale 4 Mb nonvolatile memories with heavy ions, with Co-60 gamma rays, and with a pulsed laser. These samples use silicon nanocrystals as the storage element, primarily, although some floating gate samples were also tested. Post-irradiation annealing results for the heavy ion exposures will also be reported. The heavy ion irradiations were performed using the Texas A&M University cyclotron Single Event Effects Test Facility. The chips were tested in the static mode, and in the dynamic read mode, dynamic write (program) mode, and dynamic erase mode. All the errors observed appeared to be due to single, isolated bits, even in the program and erase modes. These errors appeared to be related to the micro-dose mechanism. All the errors corresponded to the loss of electrons from a programmed cell. There were no errors which could be attributed to malfunctions of the control circuits. There was no unambiguous evidence of latchup under any test conditions, for the nanocrystal parts. Generally, the results on the nanocrystal technology compare favorably with results on currently available commercial floating gate technology, indicating that the technology is promising for future space applications, both civilian and military.

II. DESCRIPTION OF DEVICES

The test chips were experimental 4 Mb Flash EEPROM memories fabricated using 0.13 μm design rules, with NAND architecture. Nanocrystal technology is a new approach for nonvolatile memory that may eventually replace the established

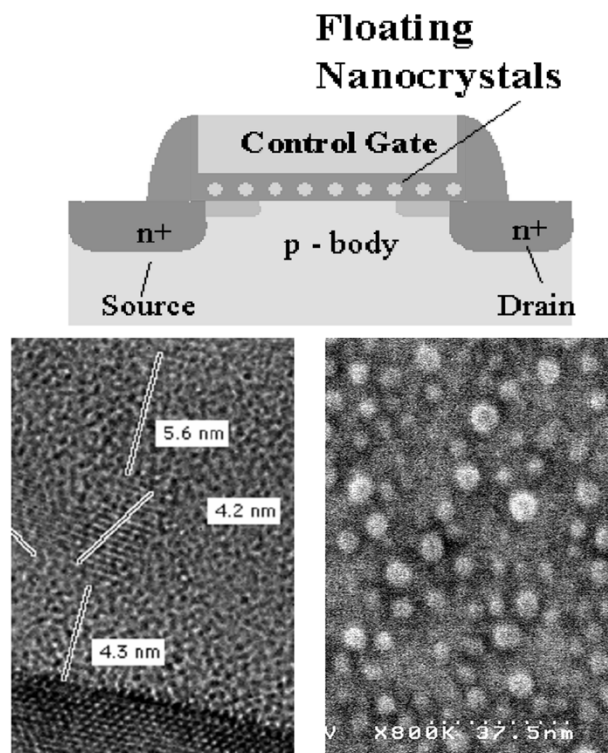


Fig. 1. Silicon nanocrystal nonvolatile memory bitcell showing the floating silicon nanocrystals used for isolated charge storage. Left photograph shows layers with different thicknesses, where nanocrystal properties can be controlled by varying deposition conditions. Right photograph is a blow-up of a single layer, indicating uniformity of nanocrystals.

floating gate technology. In this technology the storage medium consists of a layer of silicon nanocrystals, sandwiched between a bottom and a top oxide, instead of the continuous polysilicon storage medium of floating gate technology. The use of silicon nanocrystals (Fig. 1) as a storage medium is intended to provide immunity from oxide defects which can arise during program/erase operations or from radiation exposure, and to enable reduction of dielectric thicknesses and therefore lower operating voltages. These devices use channel hot electron (CHE) injection to write (that is, to add electrons to the nanocrystal array), and Fowler-Nordheim tunneling to erase (that is, to remove electrons from the array). The nanocrystals are deposited by a CVD process, where the density and diameter of the particles can be controlled by adjusting the deposition conditions. The nanocrystal technology has been described in more detail, elsewhere [1]. For these samples, the organization is 512 K \times 8, where the blocks can be programmed and addressed separately. The samples are test chips, intended to evaluate different cell

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TABLE I
IONS USED IN TESTING

Ion	E(MeV)	LET (MeV•cm ² /mg)	Range (μm)
Ar	497	8.7	175
Kr	916	29.3	117
Xe	1299	53.8	102
Au	2247	85	118

designs and cell processes, but they do not have the same peripheral circuits that might be expected in a product chip.

III. TEST PROCEDURE

The heavy ion testing was done using the Single Event Effects Test Facility (SEETF) at the Texas A&M Cyclotron, which was tuned to 15 MeV/nucleon, using the ions indicated in Table I. Each exposure was to a total fluence of 10^7 particles/cm².

The parts were tested in the static mode, in dynamic read mode, and dynamic program and erase modes. In the static testing, a pattern was written, and errors counted after the exposure. In dynamic read testing, a stored pattern was read continuously during the exposure, and the errors counted. The write or program mode was tested by continuously doing a write/read cycle. The erase mode was tested by cycling continuously through erase/write/read steps, and counting errors when the pattern read differed from the pattern expected. Patterns that could be written were all zeroes, all ones, checkerboard, and inverse checkerboard. Most of the testing was actually done with zeroes written, since that was the state sensitive to radiation. A total of nine nanocrystal parts were used in the static and dynamic testing. No floating gate parts were included in these tests. In addition, 32 nanocrystal parts and 27 floating gate parts were irradiated in the annealing studies described below. These parts were exposed, unbiased, to different ions, and returned to Freescale without any monitoring of the response on test equipment at the cyclotron. At Freescale, the threshold voltage distributions were recorded (which could not be done at the cyclotron), and monitored as a function of time and other variables. Exercising the parts before the threshold distribution was measured could have perturbed the distribution.

Total dose testing was done using the Co-60 source at GSFC. Four parts were tested, unbiased, in a Pb/Al box. This was a step-stress test, where each dose increment was between 50 and 100% of the previously accumulated dose. Dose rate was approximately 10 rad/s.

Pulsed laser testing was done at NRL, to look at effects in the peripheral circuits. The laser emits green light, which corresponds to an energy below the SiO₂ band-gap, so ionization effects in the oxides were not expected. However, the laser can be useful for studying effects due to photocurrents in the Si substrate. In the heavy ion tests, there appeared to be no effects attributable to the peripheral circuits. The purpose of the laser tests was to confirm this conclusion.

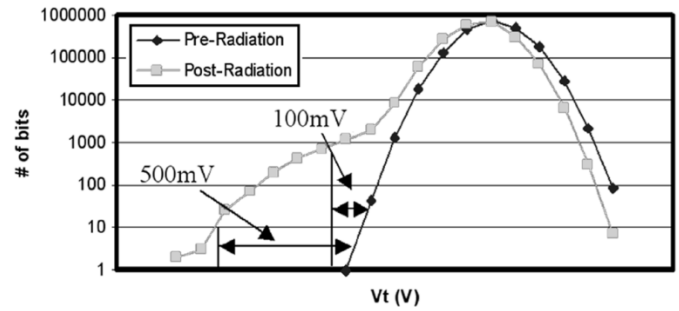


Fig. 2. Program state threshold voltage distributions pre and post radiations.

IV. RESULTS

In heavy ion testing, the errors appear to be all static bit flips, which are counted again each time the memory is read, in a dynamic read test. That is, there appear to be no errors due to transients in the peripheral circuits, even during the high voltage write and erase steps. All the testing was done at relatively low frequency (25 kHz for reading, and 5 kHz for writes), so the failure to capture any SETs may not be surprising. In addition, these samples are test chips intended to evaluate different cell designs, and do not have all the peripheral circuits a product chip might have. For example, all the different voltages needed for programming and erasing, are supplied by external power supplies. The chips do not have the capability to boost voltages on chip, as some product chips would. But previous tests of floating gate memories, reported by others [2]–[5], had shown functional interrupts (SEFI) during program and erase tests. One might expect similar results in this technology if the peripheral circuits were similar.

All the static bit flips are zeroes turned into ones in the heavy ion tests. In many of the test exposures, the cells were written as either all zeroes or all ones. No errors were observed in any of the “all ones” exposures. Under otherwise identical conditions, up to several thousand errors were observed for “all zeroes” exposures. When the cell is written into the zero state, electrons are injected into either the floating gate or the silicon nanocrystal layer. The usual effect of ionizing radiation in a MOS structure is to introduce positive trapped charge in the oxide, which reduces the net effective negative stored charge, either by compensation or by recombination. For this reason, the threshold voltage (V_T) is reduced for transistors hit by an ion. If the threshold voltage is reduced below some critical value, the bit is read as a one (gate empty of electrons) rather than as a zero (gate full of electrons).

Fig. 2 shows the tail in the threshold voltage distributions post radiation for cells written as zeroes (array full of electrons). Similar behavior has been reported on floating gate bit-cells. [6]–[8]. The test vehicle used for this experiment has special test modes, which can be used to set the fail criterion. To maximize sensitivity without introducing noise into the measurement the fail criteria during this experiment was set to 100 mV from the initial threshold distribution as shown in Fig. 2. A product would have a much wider fail margin, typically >500 mV. Fig. 2 shows that the SEU would decrease by two orders of magnitude if the fail criteria were set at a realistic target of 500 mV.

For the nanocrystal technology, the results for stored zeroes are summarized in Fig. 3. In Fig. 3 and the following figures, the

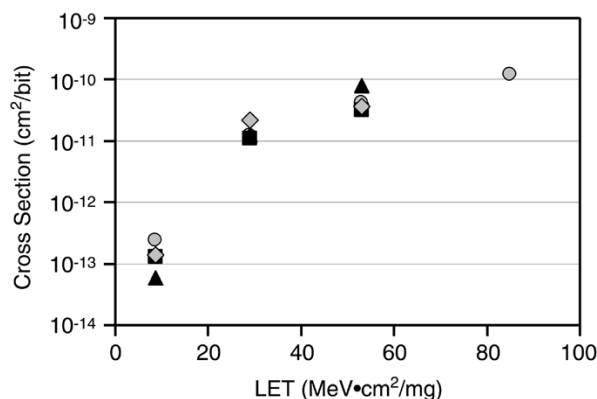


Fig. 3. Dynamic read upset cross-section.

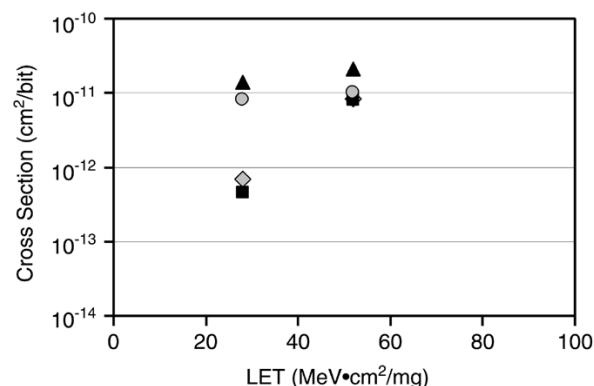


Fig. 4. Dynamic write error cross-section.

different symbols indicate different samples. For the read tests illustrated in Fig. 3, the maximum bit error count was slightly more than 10^4 , for 10^7 particles/cm². However, the area of the memory array is much less than a square cm, approximately 0.02 cm². Therefore, the number of ions hitting the array is on the order of 2×10^5 per exposure. Perhaps 30 percent of the array area is active gate area (estimated from a SEM picture), so the number of ions hitting active gate regions is about 6×10^4 per exposure. In other words, about one ion out of 6 that hits the active gate area changes the state of the cell, even at the highest LET tested so far. Therefore, the observed cross section is about one sixth times the geometric gate cross-section.

The results of the dynamic write/read testing for the nanocrystal technology are summarized in Fig. 4. The errors appear to all be static single bit errors, and the total count is less than in the read only test, because the flipped bits are being rewritten during the test, instead of being allowed to build up. No functional interrupts were observed, nor any other errors that could be attributed to the control circuits.

The results of the dynamic erase/write/read test for the nanocrystal technology are summarized in Fig. 5. Again, the errors appear to be all static single bit errors, where the total count is less than in the read only test, because the errors are being rewritten during the test. No functional interrupts were observed, nor any other errors that could be attributed to the control circuits.

No unambiguous latchup was observed in any heavy ion test, but the circuit went into a high current state after most

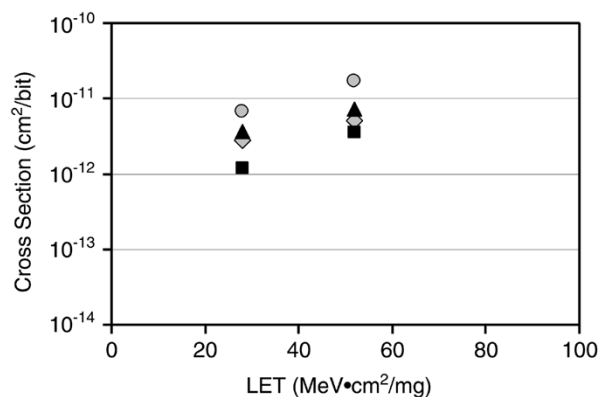


Fig. 5. Dynamic erase error cross-section.

exposures at all LETs tested. The circuit was fully functional, even in the high current state, which suggests that it was not the result of a general latchup. It is possible that there was a micro-latch somewhere on the chip, however. In laser testing, no latchup was observed on nanocrystal parts, but latchup was observed on floating gate parts. After the latchup, the floating gate circuits could not be erased or written, but they could still be read. One would expect greater latchup sensitivity in the floating gate parts, since they use higher voltages for programming and erasing.

Total dose testing was done at the GSFC Co-60 source, using parts with some bad bits pre-irradiation, unfortunately. The parts were irradiated unbiased. The dose rate was about 10 rad/sec, to a maximum dose of 200 krad, which meant the exposures lasted several hours. During a long exposure, we would expect the cells to be exercised rarely, so an unbiased exposure is reasonably representative of what the cells would really be exposed to. We note that the charge injected into the floating gate in the normal write process for these cells causes approximately a 2-V threshold voltage shift, which corresponds to a field across the oxides of at least 2 MV/cm. But this space charge field does not depend on an external bias being supplied—the parts are intended to retain information without external bias. (Typically, flash memory is intended for 10^5 or fewer write/erase cycles, with a write time on the order of ms. A hundred or a few hundred seconds spent writing a given bit, spread out over a ten year space mission, works out to a relatively small duty cycle. For this reason, the bias applied in testing is a reasonable approximation of what would be encountered in actual operation.) In the exposures, some blocks were programmed with all ones, some with all zeroes, and some with checkerboard patterns. Generally, zeroes (stored electrons) were much more sensitive than ones, because the radiation introduced positive charge. In cases where some of the bad bits pre-irradiation were ones read incorrectly as zeroes, radiation actually improved the error count. The cells are n-channel transistors, where ones have V_t below a critical value, and zeroes have thresholds above the critical value. Radiation-induced positive charge tends to lower V_t for both zeroes and ones, which increases the margin for ones, but reduces it for zeroes. One sample had a few hundred bad bits initially, but improved with dose until there were no bad bits left at 60 krad. At 100 krad, the number of bad bits was still less than the pre-rad number. The part was considered to have failed by the

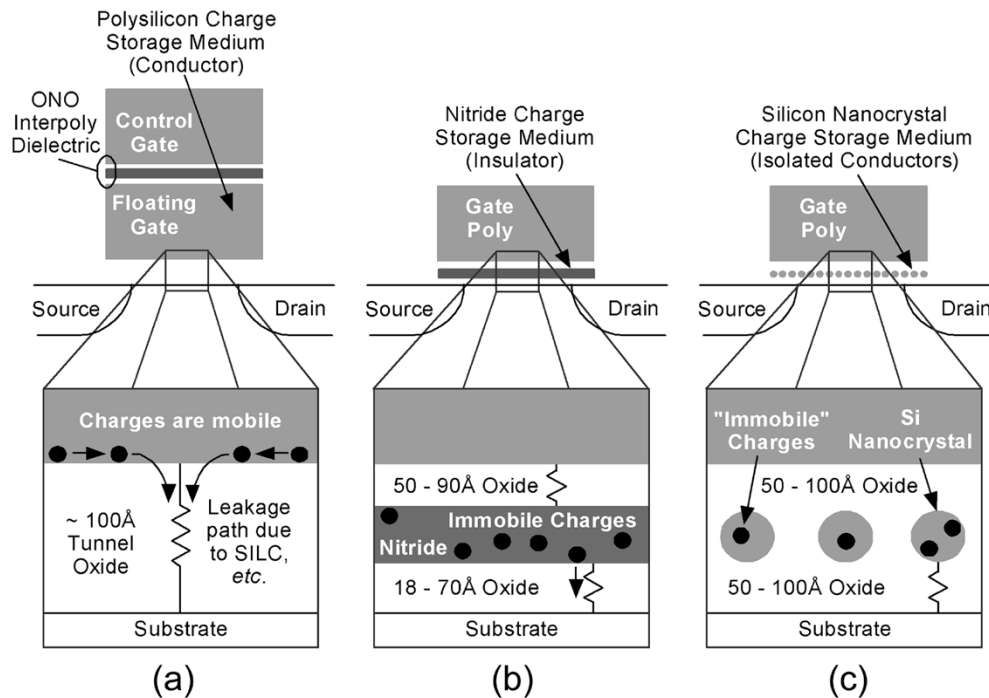


Fig. 6. (a) Floating gate. (b) SONOS. (c) Nanocrystal technology.

next data point, 150 krad, because the number of errors shot up to a few tens of thousands. The errors were due to the loss of electrons from stored zeroes. While that part was unusual in degree, multiple parts showed stable or decreasing numbers of bad ones with dose, and eventual failure due to increasing number of bad zeroes, always between 100 and 150 krad.

V. DISCUSSION

The potential advantage of nanocrystal technology is illustrated in Fig. 6. In Fig. 6(a), a leakage path, due to stress-induced oxide defects, is indicated. Because the floating gate storage element is conducting, charges move, and any leakage path drains the entire storage element. With continued scaling of the oxide thickness, it is projected that floating gate technology will have difficulty meeting its retention requirements if leakage current is on the order of one electron per day, which means that even a single oxide defect will be a critical reliability problem. On the other hand, In Fig. 6(b) (SONOS) and 6(c) (nanocrystals), the charge is not mobile, because the nanocrystals are not in electrical contact with each other, so a single leakage path drains only a small part of the array. For this reason, the nanocrystal technology is much less sensitive to oxide defects, which makes it reasonable to try to scale to thinner oxides, which, in turn, allows lower programming voltages.

Post-radiation annealing data seems to support the ideas illustrated in Fig. 6. In Fig. 7, results are shown for a floating gate device exposed to Xe ions. The threshold voltage distribution has a tail after radiation, because the bits hit by ions are shifted to the left. When the part is reset, the initial pre-radiation distribution is recovered. But when the part is allowed to anneal for 1000 hours, the tail of damaged bits reappears on the distribution. The oxide damage created by the ion is still present, and the resulting leakage path allows the charge stored on the cells to

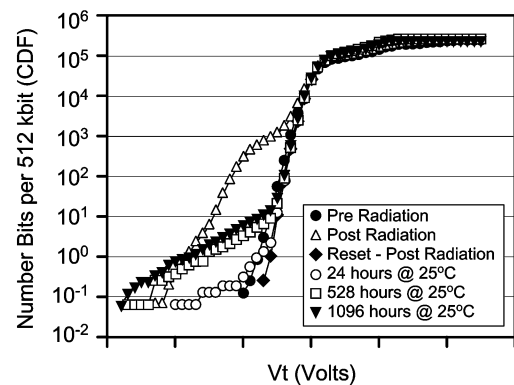


Fig. 7. Post-irradiation annealing data for floating gate sample exposed to Xe ions, then reset. Sample had also received 10 K read/write cycles before exposure.

escape, probably by tunneling from hole-trap to hole-trap. The bits with oxide damage can no longer hold a charge, and these bits would fail to meet their data retention requirements. Weak bits in the tail of the distribution are well known from electrical stress testing and from radiation exposure, and are usually attributed to oxide defects [6]–[13]. Efforts to model these effects often use percolation models, where charges move by tunneling from defect to defect [12]. It has been shown by Lelis *et al.* [14], [15], and confirmed in spectroscopic studies [16], [17], that electrons can tunnel to radiation-induced trapped holes, forming a metastable state. In response to a bias change, the electron can tunnel back to the Si substrate. But there is no reason, the electron cannot also tunnel to another trap state, if one is available. The correlation between RILC (radiation-induced leakage current) and electrical stress-induced leakage current (SILC) has been reported previously [18]. It has also been shown that heavy ion exposure can create damage—leakage paths—in thin oxides

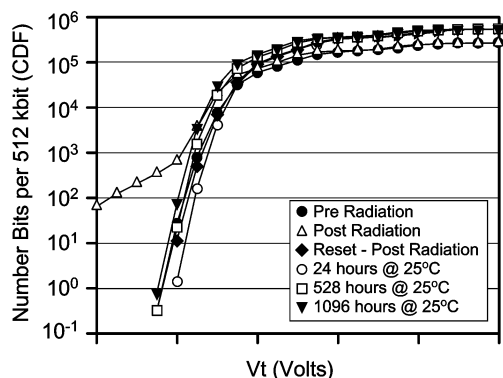


Fig. 8. Threshold voltage distribution for nanocrystal part exposed to Xe ion, with reset, and 10 K read/write cycles before irradiation.

[19], [20], and that the reliability of oxides is negatively affected by heavy ion exposure [21]. We point out, however, that the results in Fig. 7 were obtained with Xe ($\text{LET} = 53$). Similar exposures were also performed with Kr and Ar ($\text{LET} \leq 30$). For lower LET exposures, weak tail bits were not observed. Since these results extend above the iron cut off in the cosmic ray spectrum, the practical impact in space would be limited.

For nanocrystal parts, the annealing response is quite different, as illustrated in Fig. 8. After irradiation, the distribution of threshold voltages also has a tail of the bits struck by ions, and the initial pre-radiation distribution is again recovered by resetting the part. But there is no sign of the tail reappearing after 1000 hours of annealing—the nanocrystal bits with oxide damage can still hold their charge. The nanocrystal parts do meet their data retention requirements, even after an ion strike, indicating that they are less sensitive to oxide defects.

For both the floating gate and nanocrystal parts, annealing experiments similar to those shown in Figs. 7 and 8 were performed, except that the reset of the cells was omitted. For both types of device, there was no measurable change in the V_t distribution, out to 1000 hours of annealing time, which indicates little or no annealing of radiation-induced positive oxide charge.

The underlying mechanism for the bit errors appears to be related to the micro-dose—an ion deposits a small, dense cluster of positive charge, which neutralizes enough of the stored electrons on the storage element to change the state of the cell, either through recombination or compensation. This mechanism has been described most completely for normal gate oxides [22], [23]. However, Cellere *et al.* [7] have previously reported that the negative charge lost off floating gate devices irradiated with heavy ions was far greater than the amount of positive charge deposited by an ion. In one case, they calculated a loss of about 2800 electrons from the floating gate, compared to an estimate of about 70 positive charges deposited directly by the ion (based on analysis in [24]). They discussed three different possible models for this anomalous charge loss, which they referred to as 1) positive charge assisted leakage current (PALC), 2) conductive pipe model, and 3) the electron emission model. Ultimately they concluded that, although each model had some points to recommend it, none was fully satisfactory. In our experiments, the situation is somewhat different, because the cells are more highly scaled. The cell area is about an order of magnitude less than for the samples reported by Cellere *et al.*, but

the ion-induced threshold voltage shift is about the same, which means the number of electrons lost is about an order of magnitude less. In addition, there are at least two sources of uncertainty involved in the estimate of 70 positive charges deposited. First, the threshold voltage in programmed cells is about 2-V higher than in unprogrammed cells. This means that the stored electrons induce a field of 2×10^6 V/cm across a 10 nm tunnel oxide, and also across a 10 nm control gate oxide. When the gate is unbiased, which is the usual condition, the field would cause positive charge to move to the floating gate from both oxides, which would double the estimate of the charge deposited. Second, there has never been a careful measurement of the yield of charge as a function of applied field at the LET relevant in these experiments. The closest result in the literature was reported by Stapor *et al.* [25], where the experimental yield was, in fact, about 1%, as assumed in [7]. But the highest applied field in that work was less than 1 MV/cm, compared to 2 MV/cm here, and it is well known that the yield increases with increasing field. Also, the agreement between the model and the experiment in [25] was less than perfect, so scaling the experimental results is not a simple task. We estimate for our nanocrystal samples, a threshold shift of 1 V corresponds to a loss of 350–400 electrons. If we have charge collection from both oxide layers, and the yield is assumed to be 2%, we calculate about 300 positive charges are deposited by the ion. These numbers are essentially in agreement, within the known uncertainties. Therefore, direct deposition of positive charge by the incident ion should not be ruled out as the controlling mechanism, for devices scaled beyond a certain point. Certainly, for the next technology node, 90 nm as opposed to 130 nm for our samples, the cell area will only be half as great, and the charge to produce a 1-V V_t shift will also be reduced by half, if the oxide thickness stays the same. Then the charge loss from the cell from an ion hit will be less than the charge deposited by the ion.

On the other hand, for our nanocrystal samples, for our floating gate samples, and for the older floating gate technology reported in [7], the threshold voltage shift induced by similar ions is about 1 V in all cases, even though the amount of charge flowing differs widely in some of the cases. This seems to argue for a circuit modeling approach to the problem—there is a voltage driving a current through an impedance, initially. When the voltage drops to a certain point, the current flow stops. The three models proposed in [7] all fit this framework. However, the fact that the threshold shift induced by ions is the same in the nanocrystal and floating gate parts, seems to be inconsistent with one of the models, the conducting pipe model. The reasons for this conclusion have already been discussed, in connection with Fig. 6. But the other two models in [7], electron emission and PALC seem to predict the same response for nanocrystal and floating gate devices, consistent with our results. We conclude that there is still no clear choice for a model to explain heavy ion effects on flash memory cells—none of the candidates proposed so far is fully satisfactory.

VI. CONCLUSION

All the radiation-induced errors in this work are due to the loss of stored electrons from the nonvolatile storage element.

In the nanocrystal arrays, the cells can be reset after an error is detected, and they have no apparent long-term damage. Floating gate cells, on the other hand, do have long-term permanent damage after being struck by a heavy ion. The cells can be reset successfully, initially, but they have enough leakage current that many of them will no longer meet their data retention requirements. A few possible theories have been proposed for the degradation in data retention performance of radiated floating gate bit-cells [7], [8], based on localized damage to the oxide, which creates a path for leakage current.

The basic nanocrystal technology looks promising for space applications, since many of the effects observed in other non-volatile memory technologies have not been observed. All the errors so far appear to be related to micro-dose effects in single cells, and the sensitivity is determined by the voltage margins, rather than any intrinsic characteristic of the underlying technology.

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